

# FLIR ISC1105™

## X-Ray Readout Integrated Circuit

FLIR's readout integrated circuit (ROIC) standard product line now includes the ISC1105 256 x 1 channel chip on flex (COF) as well as an Evaluation Board for testing the device parameters and customers' detector panels. The ISC1105 COF is designed for applications including digital radiography, mammography, surgery, fluoroscopy, angiography, tomography, nondestructive testing and industrial instrumentation.

### Now available: Chip on Flex and Evaluation Board

*Ideal for X-ray medical imaging applications due to their flexible architecture, simple interfaces, and compatibility with various flat panel arrays and detectors materials.*

### Key Features

- Designed for use with Selenium, Cesium Iodide, Silicon, Amorphous Silicon, Gallium Arsenide, and Cadmium Zinc Telluride detectors
- Adjustable parameters for integrator gain selection, low-pass filter time constant, integration mode, ADC resolution, and readout direction
- Designed for abutting multiple chips to read out large flat panel X-ray detectors
- Turn-key COF solution
- ROIC parameter and detector panel evaluation

### Delivery Options

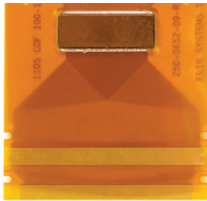
- Bare ROIC devices are delivered in wafer form, probe tested, and labeled according to pass/fail criteria.
- ROIC devices mounted on flex, fully tested and delivered in trays
- Evaluation board with 2 plug in 100µm pitch COF devices
- All deliveries include user interface documentation

### Custom Design

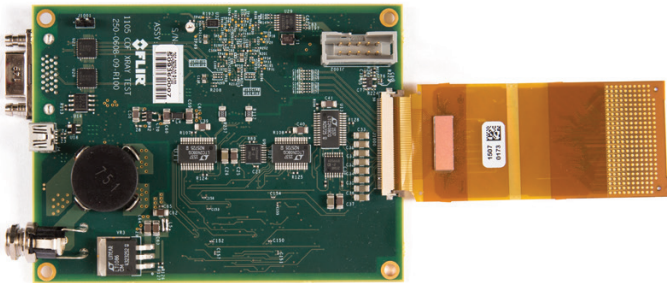
*If our standard ROIC products do not meet your requirements, FLIR offers full custom design services, from trade study through design and fabrication of ROICs and COFs.*



Evaluation Board with Cover



Chip on Flex



Evaluation Board

# Specifications

ROIC Parameter	ISC1105		
Input DC Offset	1.0 to 2.6 V (nominal 1.2 V)		Adjustable integrator DC operating point
Carrier Collected	Electrons, Holes		
Input Charge Handling (Normal operation)	≥ 15 pC		
Input Charge Handling (Reset)	≥ 200 pC		
Readout Noise	ENC ≤ 500 e <sup>-</sup> (C <sub>INT</sub> = 0.25 pF, C <sub>DET</sub> = 50 pF, ΔV <sub>INT</sub> = 2 V, tau = 5.2 μs, 16 bit)		Does not include system or detector contributions
Readout Noise	ENC ≤ 5000 e <sup>-</sup> (C <sub>INT</sub> = 8.00 pF, C <sub>DET</sub> = 50 pF, ΔV <sub>INT</sub> = 2 V, tau = 5.2 μs, 16 bit)		
Integrator Gain Control	C <sub>INT</sub> = 0.25 pF – 8.0 pF, 0.25 pF increments, FSC = 0.5 pC – 16 pC		
LPF Time Constant	1.2 μs – 11 μs ±30%, 3 bits, -1.4 μs/step		
ROIC Crosstalk	≤ 0.25%		
PSRR	≥ 40 dB at ≤ 250 Hz		
# Of Channels	256		
Channel Pitch	50 μm		
ADC Resolution	12 - 16 bits		
Operating Temperature	10°C – 70°C		At ROIC
Power Dissipation	≤ 1.5 mW/channel – default ≤ 3.0 mW/channel – max front end ≤ 0.1 mW/channel – sleep mode		
Clock Frequency	128 MHz		
Minimum Line Time	18 μs (12 bit ADC) 34 μs (13 bit ADC) 66 μs (14 bit ADC) 130 μs (15 bit ADC) 258 μs (16 bit ADC)		
Input Biases	VPOS, VPOSINT 3.6 V VNEG, VNEGINT 0.0 V VPOSR 3.6 V VNEGR 0.0 V VNEGADC 0.0 V VPOSD 3.6 V VPD 1.8 V VND 0.0 V VREF_INT 1.2 V (nom) 2.5 V (nom) VREF_CDS 0.5 V (nom) 2.25 V (nom) VREF_ADC 0.5 V (nom) VREF_RAMP 3.1 V (nom)		Analog Positive Analog Negative Analog Positive (for ramp circuitry) Analog Negative (for ramp circuitry) Common Reference for Ramp, T/H Digital Positive Digital Positive Digital Negative Integrator Reference (electron collection) Integrator Reference (hole collection) CDS Reference (electron collection) CDS Reference (hole collection) ADC Reference Ramp Gain Adjust
Input Clocks	Name      VIC      VID CLK        0.9 V    0.15 V SYNC      0.9 V    0.15 V DATA     0.9 V    0.15 V INJCLK    0.9 V    0.15 V		VIC range: 0.7 - 1.3 V, VID range: ≥ 0.05 V Master Clock Sync Mode Control Injection Clock Control
Channel Nonlinearity	≤ 0.5%, From 0% to 92%		
Offset Stability	< 0.5 LSB/°C, CINT = 4 pF, 14 bit LSB		
Outputs	2 Digital, sub-LVDS interface		2 pads per output
Digital Readout Rate	128 MHz		256MHz data throughput rate
Die Size	15.0 mm x 5.0 mm		

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 17-0740-OEM