Neutrino, Electrical Interface Description Document (IDD)

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The information herein does not contain technology as defined by the EAR, 15 CFR 772, is publicly available and therefore not subject to the EAR.

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1 Document

1.1 Revision History

Version	Date	Comments
100	12/09/2013	*Initial release*
110	08/13/2013	*Changed DSE to Neutrino, corrected ITAR level2 statement*
111	09/17/2018	*Changed ITAR statement to EAR*

1.2 Scope

Neutrino is a miniature cryogenically cooled infrared sensor core from FLIR Systems®.

This Interface Description Document (IDD) defines the electrical interface requirements for the product. Controlling Neutrino is described in the Neutrino Software Interface Description Document, and more user friendly control using Camera Controller GUI is describe in Neutrino User Guide.

2 Applicable Documents

The following documents form a part of this specification to the extent specified herein.

2.1 FLIR Systems Documents

102-2001-61	Neutrino Software Interface Description Document
425-0025-00-10	Neutrino Users Guide

2.2 External Documents

ANSI/TIA/EIA-232 (formerly RS232)	Interface Between Data Terminal Equipment and Data Circuit-Terminating Equipment Employing Serial Binary Data Interchange
ANSI/TIA/EIA-644	Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits
AIA Camera Link	Need real doc number, but National Semi and others have good description of the protocol

3 Electrical Interface Requirements

This document defines requirements for the following interfaces:

- Power
  - Input power
- Digital video data
  - Parallel channel (single-ended)
  - Camera Link
- External Sync Interface
- Communication interface

3.1.1 Interface Connectors

3.1.1.1 Neutrino Logic Interface Connector

The electrical interface to Neutrino logic is via a single high-density 50-pin connector: Hirose #DF12-50DS-0.5V(86). The recommended mating connector is Hirose #DF12(5.0)-50DP-0.5V(86) for a mating stack height of 5mm.

The pin and the signal names are shown in Table 1. See Figure 1 for a picture showing the physical pin numbering of the connector.

Specifically, the signals are grouped into one for four:

a. Serial Communication
b. Camera Link digital data out
c. Parallel digital data out
d. External sync and reset
e. Power

Table 1: Primary I/O Connector Pin Definition

Pin #	Signal Name	Pin #	Signal Name
1	COMM_TX (RS232_TX)	2	COMM_RX (RS232_RX)
3	LINE_VALID_OUT	4	FRAME_VALID_OUT
5	DGND	6	DGND
7	CAMLINK_CLKP	8	CAMLINK_CLKN
9	CAMLINK_DATA0P	10	CAMLINK_DATA0N
11	CAMLINK_DATA1P	12	CAMLINK_DATA1N
13	CAMLINK_DATA2P	14	CAMLINK_DATA2N
15	CAMLINK_DATA3P	16	CAMLINK_DATA3N
17	DGND	18	DGND
19	n/c	20	DATA_OUT13
21	EXTERNAL_SYNC	22	DATA_OUT12
23	DATA_OUT11	24	DATA_OUT10
25	DATA_OUT9	26	DATA_OUT8
27	DGND	28	DGND
29	DATA_OUT7	30	DATA_OUT6
31	DATA_OUT5	32	DATA_OUT4
33	DATA_OUT3	34	DATA_OUT2
35	DATA_OUT1	36	DATA_OUT0
37	DGND	38	DGND
39	CLOCK_OUT	40	n/c
41	DGND	42	DGND
43	n/c	44	n/c
45	DGND	46	n/c
47	MAIN_PWR_RTN	48	MAIN_PWR
49	MAIN_PWR_RTN	50	MAIN_PWR

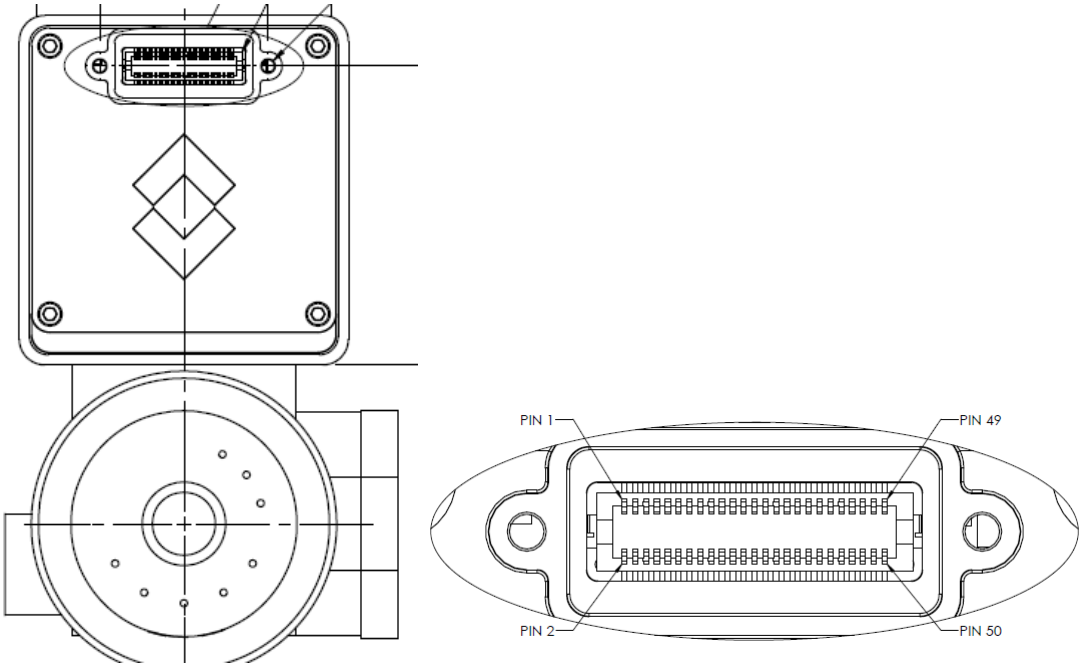

Figure 1: Primary I/O Connector Pinout, Hirose #DF12-50DS-0.5V(86)

3.1.2 Power Interface

Two DC power supplies are required for the Neutrino unit as tabulated in **Error! Reference source not found.**.

a. Neutrino provides full functionality when voltage as specified in **Error! Reference source not found.** is applied across MAIN_PWR and MAIN_PWR_RTN of the 50 pin connector and across the RED and BLACK pig tail wires of the cooler controller.

b. For 5V DC input voltage between the minimum value and the shutdown value specified in **Error! Reference source not found.**, Neutrino behavior is undefined.

c. +5VDC and the Cooler Power are fully isolated from each other, but consideration should be given to minimize the ground difference between the two to less than 1V.

Note: Neutrino does not provide internal protection against reverse-voltage or over-voltage.

Table 2 Neutrino Input Power Requirement

Parameter	min	nominal	max	Notes
+5V DC Logic 50 pin connector across MAIN_PWR and MAIN_RTN	4.9V	5.0V	5.5V	*Voltage in excess of this value may cause permanent damage to the DSE.*
+5V DC Power Dissipation	1.5W		2.2W	
+5VDC shutdown Voltage		4.5V		
Cooler Power. Red and black pigtails	9V DC	12V DC	35V DC	*Transient protection but not reverse voltage protection*
Cooler Power Dissipation	2W	3W	14W	

3.1.3 Digital Interface

Four different digital interfaces are used to communicate with the sensor.

3.1.3.1 Serial Communication Interface

The serial communication interface conforms to the industry standard serial RS-232C standards with the exception of the logic level and polarity.

BAUD rate is 57.6K, one start, 8 bit one stop format. DSE does not send out autonomous communication packet, as such, the serial interface can be considered half-duplexed.

Neutrino uses “LVTTL” format of the serial interface. LVTTL is after the Rx receiver /before the Tx transmitter. As such;

a) the signal levels are from 0V to 3.3V, 5V compatible
b) Space is logic low and the Mark is logic high. (inverted from standard RS232C logic levels)

3.1.3.2 Digital Data Channels

Neutrino provides two digital transmit channels, one parallel and one serial. Each output can be enabled or disabled independently.

NOTE: Neutrino is designed to be an integral part of the host system; as such the I/O drivers were designed for 24 inch maximum drive capability.

3.1.3.2.1 Parallel Digital Data

Neutrino provides the option of a digital data protocol resembling that of a typical CMOS camera. Specifically:

a) The parallel channel consists of a clock, 14 parallel bits of data, a line-valid and a frame-valid signals. See **Error! Reference source not found.** for pin assignments.

b) The channel utilizes 3.3V CMOS logic levels.

Line timing is depicted in

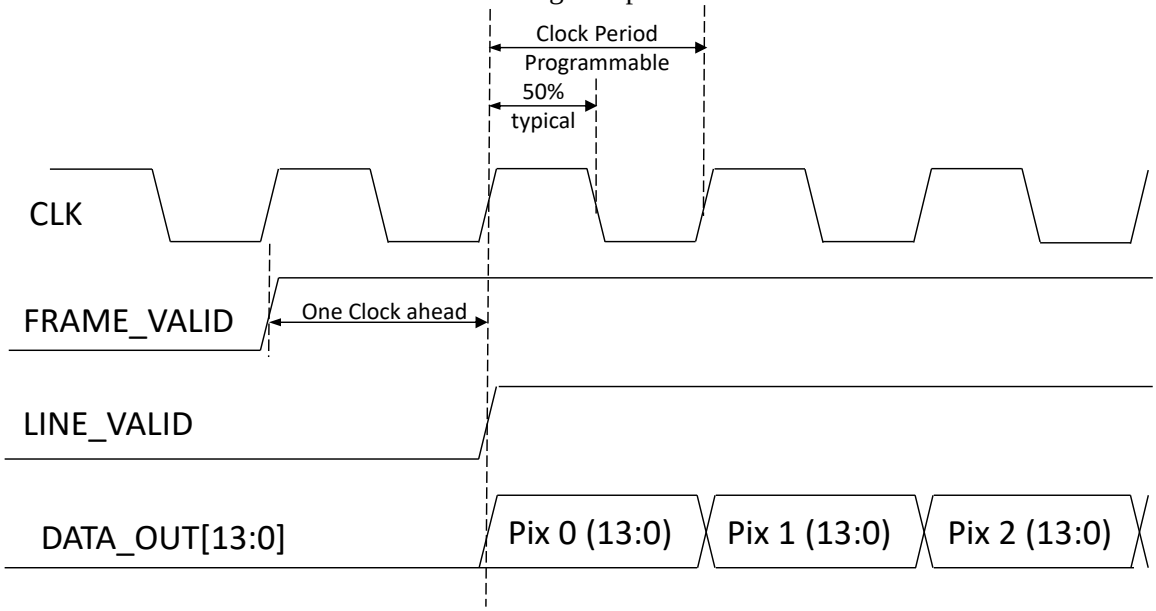

Figure 2 Line Timing

c) . The clock rate is based on the DSE FPA timing parameters and is 2 times the FPA_CLK rate times the number of channels.

End of line and end of frame timing is depicted in

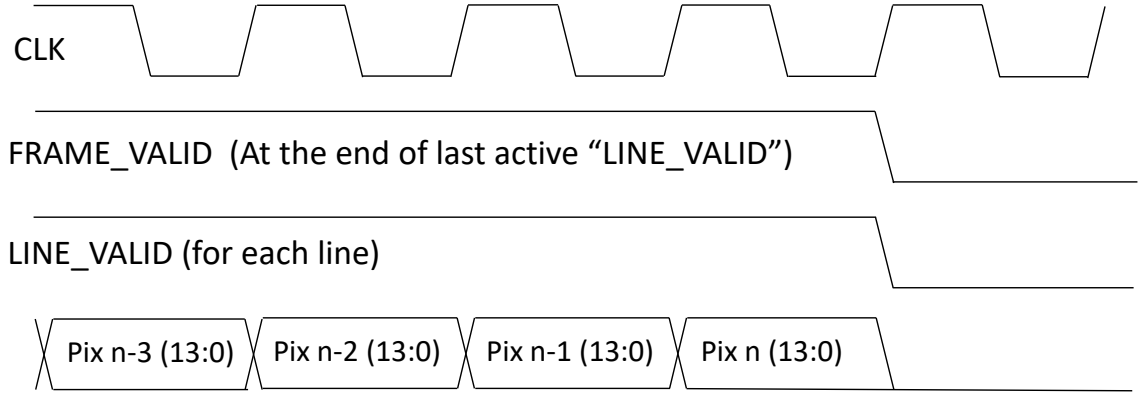

Figure 3 End of Active Frame Timing

d) .

e) Neutrino changes data and controls at the positive edge. *It is highly recommended that the receiving logic use the negative edge of CLK to latch the parallel data and controls.*

f) Clock, Frame_Valid and LINE_VALID are configurable and dependent on DSE setting.

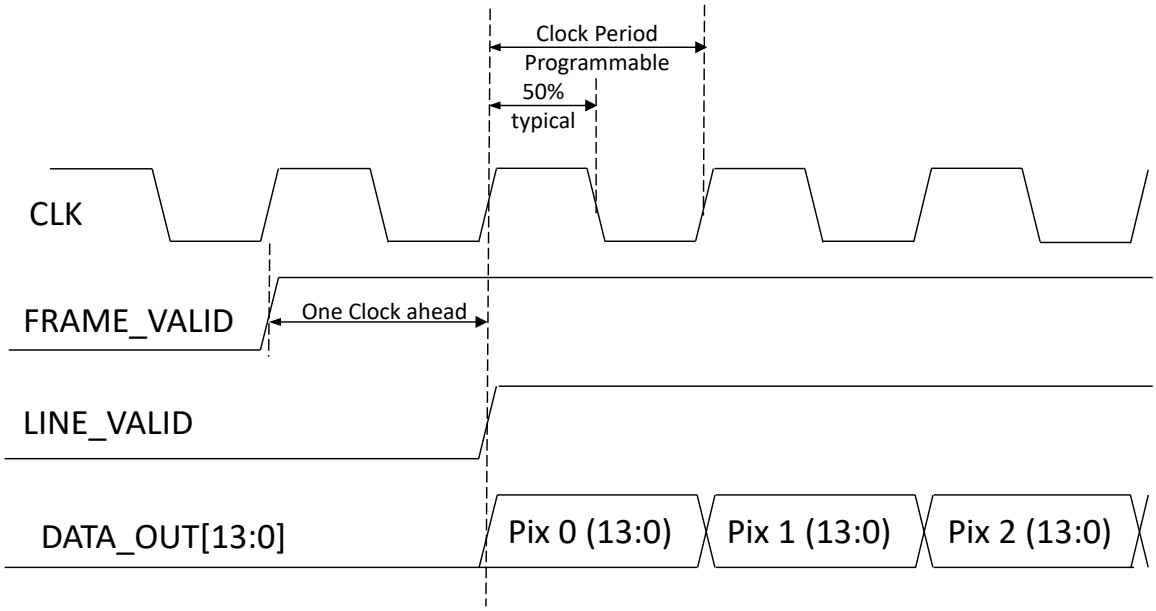

Figure 2 Line Timing

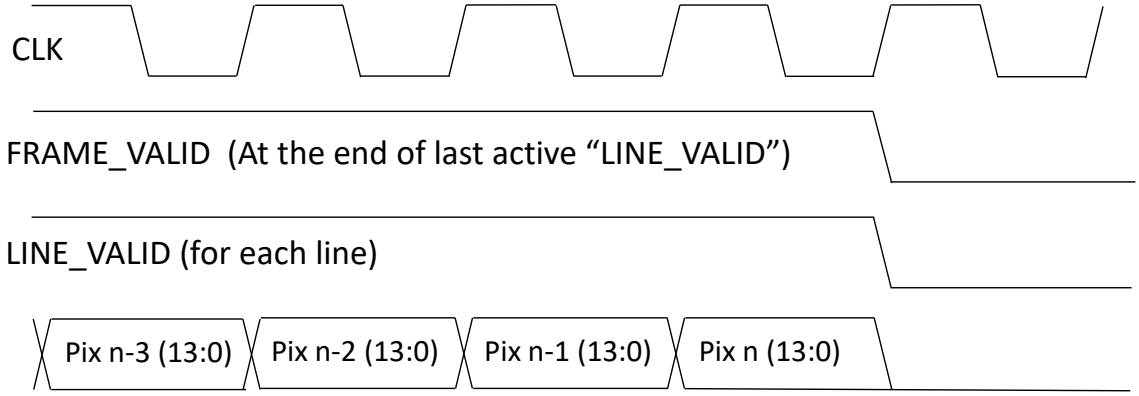

Figure 3 End of Active Frame Timing

3.1.3.3 Camera Link Serial Digital Data

Neutrino provides the option of Camera Link digital data:

1. Per Camera Link, base configuration.
2. The clock rate and the frame rate depend on the DSE setup parameters.
3. Requires 100 ohm differential termination at the receiver.

3.1.4 Frame Synchronization Interface

Neutrino can be slaved to an external sync (host). Using the external sync input allows the "host" to synchronize the FPA operation.

External sync pulse must be greater than 1usec wide. Neutrino can be set to use the positive or negative edge, but not both. The voltage levels are 0V to 3.3V.

When Neutrino is in the free run mode, EXT_SYNC_IN signal is ignored.

3.1.5 External Reset (not used at Neutrino assembly level)

4 Neutrino Cryo Cooler Controller

The MWIR FPA resides in an evaluated dewar and is cooled using FLIR's MC3 integral Sterling cycle cyro engine.

The cryo-engine uses 3 phase DC brushless motor and control electronics to drive the motor and regulate FPA operating temperature with a feedback loop using a temperature sensor located next to the FPA. Nominal operating temperature is factory set at 77 Kelvin. Variation in the set point is less than +/-2 Kelvin over the operating temperature range.

The cryo cooler is an independent module and is independent of Neutrino electronics. The cryo cooler will initiate cooling once 12V is applied.

As noted in section 3.1.4, Table 4, the cryo cooler electronics will operate from 9VDC to 35VDC to accommodate wide range of "host supplies" but 12VDC is recommended.