FLIR ISC0905: 640 x 512, 30µm Two Color ROIC

Specification

January 13, 2012

- **Version 1.00: January 13, 2012**
  – Initial Release

ISC0905 Specification and Requirements Review (1 of 5)

ROIC PARAMETER	SPECIFICATION REQUIREMENT	COMMENTS
Array Configuration	640 x 5 12	
Pixel Pitch in Columns (1024)	30 µm	
Pixel Pitch in Rows (1024)	30 µm	
Input Polarity	Selectable P-on-N (Current Flows into Inputs) & N-on-P (Current Flows out of Inputs)	Color Selectable on a per frame basis SLS, InSb, InGaAs, HCT
Detector Bond Pad	1 (6 µm x 6 µm) pad opening per pixel, plus detector common pad ring around cell array	One indium bump connection per pixel. Additional detector common pad ring of 6 pixels around the array of 640x5 12 for a total array of 652x524
Test Detector Pads	4 pads to test individual detectors	Maintain similar pixel locations as the ISC9803
Input Configuration	Direct Injection (DI)	
Core Multiplexing Configuration	Voltage Mode	

Detector Impedance (RrAd) at 77K	> $1x10^3$ (Ohm-cm^2)	Impedance at reverse bias operating point. Used for Performance Analysis, Prediction and Simulation

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ROIC PARAMETER	SPECIFICATION REQUIREMENT	COMMENTS
Detector Capacitance	≤0.6pF	Used for Performance Analysis Prediction and Simulation
Temperature of Operation	65K – 300K	Estimated Room Temperature Operation will have reduced performance
Input Biases	VDETCOM 0-5.5V VPOS 5.5V VPOSOUT 5.5V VPD 5.5V VOUTREF 1.55V - 4.N VNEG O.OV VNEGOUT O.OV VND O.OV	Detector Common (optional) Analog Positive Output Positive Digital Positive Analog Reference;P-on-N 1.55V; N-on-P 4.*N* Analog Negat ive Output Negative Digital Negative
Input Clocks	Name Vhigh to Vllow CLK VPD to VND LSYNC VPD to VND FSYNC VPD to VND DATA VPD to VND RESET_B VPD to VND	Master Clock Line Sync Frame Sync (Integ Control) Mode Control Master Reset (optional)
Input Clock Rise and Fall	10% to 90% in 5nS	

Outputs	Selectable 4 or 8 with Reference Output	
Output Interface	≥ 100k Ohms ≤ 12 pf	12pF includes capacitive load up to and including wire-bond to ROIC pad

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ROIC PARAMETER	SPECIFICATION REQUIREMENT	COMMENTS
Output Voltage Swing	2.5V ± 0.2V (Baseline P-on-N ~1.55V ± 0.1V) (Baseline N-onP ~4N ± 0.1V)	Default settings -2.5V ± 0.2V typical output range at 77K Estimated range for OBV reverse detector bias Output swing dependent on reverse bias
Power	8 Outputs 330mW 4 Outputs 235mW	Full frame operation at 18MHz output data rate and T=77K
Control Register Functions	Programmable Test 1/0 Anti-Blooming Control Power Control Master Current Detector Bias Adj. Invert / Revert Windowing (programmable size and position) 4 or 8 Outputs Reference Output Enable Adjustable Timing Edges Global Reset Pixel Color Select	

Programmable Test	Test Row Input Unit Cell Test Injection VET Circuit	
Detector Bias Adjust (P on N)	0mV to -800rnV Adjustment @ nominal current (1nA)	~8mV bit bias control per color
Detector Bias Adjust (N on P)	0mV to +800mV Adjustment @ nominal current (1nA)	~8mV bit bias control per color

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ROIC PARAMETER	SPECIFICATION REQUIREMENT	COMMENTS
Detector Bias Uniformity	<20mV 1-theta	Dependent on Process Vt Uniformity Measured ISC9705 1-sigma of approximately 7mV,expect similar performance from ISC0905
Integration Mode	Snap Shot ITR & IWR	Integrate one color per frame
Integration Time	>100µs to 0.9*full frame Adjustable on a per frame basis	For 240HZ → 4.167ms full frame → 3.75ms max tint Lower Tint estimated, it is possible to program Tint to <100µs, but integrated output may be nonlinear and limited.
Total Input Current Min Nominal Max	20pA 1nA 10nA	Simulation Range includes signal and dark current
Input Charge Handling	≥ 18 x 10^6 carriers	Can reduce well size with minimal layer changes
Non-Linearity	< ± 2% from least squares line fit	Output Voltage vs.Tint Max deviation from least squares fit over 15% to 85% of full range
Noise	≤ -80dB of Full Well (Input Referred) At Maximum Readout Rate	Without Detector or System Noise ROIC Noise in dB defined as 20*log (noise e- / full well e-)

ISC0905 Specification and Requirements Review (5 of 5)

ROIC PARAMETER	SPECIFICATION REQUIREMENT	COMMENTS
Column Output Order-8 Output A : Output H	Column 0,8,...,632 : Column 7,15,...,639	Eight Output Mode Normal Readout Direction
Invert / Revert	Reverse Order of Rows and/or Columns	Select using Control Register
Temperature Sensor	0.7V ± 0.05V @ 300K 1.070V ± 0.05V at 77K	Test/Temp Pad
Full Frame Rate Pixel Rate 18MHz & T=77K unless otherwise noted	8 Output 240 FPS 4 Output 120 FPS	9MHz ISC0905 input clock For 512x512 windowed array Warm operation will have slower frame rate
Data Valid / Settling Time	Settle to 0.1% @ T=77K in ≤45ns	12pF // 100k0 load Default power settings;10ns Data Valid Warm operation requires longer settling time
Adjacent ROIC Pixel Crosstalk	< 0.1% @ T=77K < 1.0% @ T =300K	Limited routing and system impedance
Non-Adjacent ROIC Pixel Crosstalk	< 0.1% @ T=77K 8 output < 1.0% @ T=300K 8 output	Limited routing and system impedance

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Color-Color ROIC Pixel Crosstalk	< 0.1% @ T=77K < 1.0% @ T=300K	Limited routing and system impedance
Minimum Window Size and Resolution	32 columns x 8 Rows 64 columns x 8 Rows	4 Output Mode 8 Output Mode
Die Size	< 23mm x 21mm	To edge of scribe lane. Die extent to fit within the extent of the reticle exposure area.
Pad Layout	Maximizing commonality with ISC0903	Match with ISC0903 as much as practical given the array size