

**ISC0904: 1k x 1k
18 μ m N-on-P ROIC**

Specification
January 13, 2012

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The World's **Sixth Sense**[™]

FLIR ISC0904: 1k x 1k, 18µm N-on-P ROIC

- **Version 1.00: January 13, 2012**
 - Initial Release



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ISC0904 Specification and Requirements Review (1 of 5)

ROIC PARAMETER	SPECIFICATION REQUIREMENT	COMMENTS
Array Configuration	1024 x 1024	
Pixel Pitch in Columns (1024)	18 µm	
Pixel Pitch in Rows (1024)	18 µm	
Input Polarity	N-on-P (Current Flows out of Inputs)	SLS, InSb, InGaAs, HCT
Detector Bond Pad	1 (6 □m x 6 □m) pad opening per pixel plus detector common pad ring around cell array	One indium bump connection per pixel. Additional detector common pad ring of 6 pixels around the array of 1024x1024 for a total array of 1036x1036.
Test Detector Pads	4 pads to test individual detectors	Maintain similar pixel locations as the ISC0404
Input Configuration		Direct Injection (DI)
Core Multiplexing Configuration		Voltage Mode

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Detector Impedance (RrAd) at 77K	$> 1 \times 10^3$ (Ohm-cm²)	Impedance at reverse bias operating point. Used for Performance Analysis, Prediction and Simulation
Detector Capacitance	≤ 0.2 pF	Used for Performance Analysis, Prediction and Simulation
Temperature of Operation	65 K-300 K	Room Temperature Operation Will Have Reduced Performance.

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ISC0904 Specification and Requirements Review (2 of 5)

ROIC PARAMETER	SPECIFICATION REQUIREMENT	COMMENTS																		
Input Biases	VPOS 3.6 V VPOSOUT 3.6 V VPD 3.6 V VNEG 0.0 V VNEGOUT 0.0 V VND 0.0 V VOUTREF 3.4 V	Analog Positive Output Positive Digital Positive Analog Negative Output Negative Digital Negative Analog Reference (Optional: Internal or external reference)																		
Input Clocks	<table border="0"> <tr> <td><u>Name</u></td> <td><u>Vhigh to Vlow</u></td> <td><u>CLK</u></td> </tr> <tr> <td></td> <td>VPD to VND</td> <td></td> </tr> <tr> <td>LSYNC</td> <td>VPD to VND</td> <td></td> </tr> <tr> <td>FSYNC</td> <td>VPD to VND</td> <td></td> </tr> <tr> <td>DATA</td> <td>VPD to VND</td> <td></td> </tr> <tr> <td>RESET_B</td> <td>VPD to VND</td> <td></td> </tr> </table>	<u>Name</u>	<u>Vhigh to Vlow</u>	<u>CLK</u>		VPD to VND		LSYNC	VPD to VND		FSYNC	VPD to VND		DATA	VPD to VND		RESET_B	VPD to VND		Master Clock Line Sync Frame Sync (Integ. Control) Mode Control Master Reset (optional)
<u>Name</u>	<u>Vhigh to Vlow</u>	<u>CLK</u>																		
	VPD to VND																			
LSYNC	VPD to VND																			
FSYNC	VPD to VND																			
DATA	VPD to VND																			
RESET_B	VPD to VND																			
Input Clock Rise and Fall	10% to 90% in 10 ns																			
Outputs	Selectable 4, 8 or 16 with Reference Output																			
Output Interface	≥ 100 kOhms ≤ 15 pF	15 pF includes capacitive load up to and including wire-bond to ROIC pad																		

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Output Voltage Swing	2.3 V \pm0.2 V (Baseline ~ 3.4 V \pm0.1 V)	Default settings: ~2.4 V typical output range at 77K ~2.3 V typical output range at 300K



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ISC0904 Specification and Requirements Review (3 of 5)

ROIC PARAMETER	SPECIFICATION REQUIREMENT	COMMENTS
Power (12.5 MHz output data rate and T = 77 K unless otherwise noted)	4 Outputs ≤ 72 mW 8 Outputs ≤ 95 mW 16 Outputs ≤ 130 mW	Power requirements for maximum window size
Control Register Functions	Programmable Test I/O Anti-Blooming Control Power Control Master Current Detector Bias Adj. Invert/Revert Windowing (programmable size and position) 4, 8 or 16 Outputs Integration Mode (ITR, IWR, NDRO) Reference Output Enable Global Reset	
Programmable Test	Test Row Input Unit Cell Test Injection VET Circuit	

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Detector Bias Adjust (N on P)	0 mV to -800 mV Adjustment @ nominal current (1 nA)	7 bit bias control
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ISC0904 Specification and Requirements Review (4 of 5)

ROIC PARAMETER	SPECIFICATION REQUIREMENT	COMMENTS
Integration Mode	Snapshot ITR and IWR	
Total Input Current Min Nominal Max	20 pA 1 nA 10 nA	Simulation range, includes signal and dark current
Input Charge Handling	$\geq 7 \times 10^6$ carriers	
Non-Linearity	$< \pm 2\%$ from least squares line fit	Output Voltage vs. Tint Max Dev. from least squares fit over 15% to 85% of full range
Noise	≤ -76 dB of Full Well (Input Referred) At Maximum Readout Rate	Without Detector or System Noise. ROIC noise in dB defined as $20 \cdot \log(\text{noise } e^- / \text{full well } e^-)$
Column Output Order-4 Output A : Output D	Column 0,4,...,1020 : Column 3,7,...,1023	Four Output Mode Normal Readout Direction
Column Output Order-8 Output A : Output H	Column 0,8,...,1016 : Column 7,15,...,1023	Eight Output Mode Normal Readout Direction

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Column Output Order-16 Output A : Output P	Column 0,16,...,1008 : Column 15,31,...,1023	Sixteen Output Mode Normal Readout Direction
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ISC0904 Specification and Requirements Review (5 of 5)

ROIC PARAMETER	SPECIFICATION REQUIREMENT	COMMENTS
Invert / Revert	Reverse Order of Rows and/or Columns	Select using Control Register
Temperature Sensor	0.7 V ± 0.05 V @ 300 K 1.070 V ± 0.05 V at 77 K	Test/Temp Pad
Full Frame Rate (Pixel Rate 12.5 MHz and T = 77 K unless otherwise noted)	4 Output ≥ 30 FPS 8 Output ≥ 60 FPS 16 Output ≥ 120 FPS	
Data Valid / Settling Time	Settle to 0.1% @ T=77 K in ≤ 55 ns	15 pF // 100 kΩ load Default power settings
Adjacent ROIC Pixel Crosstalk	< 0.1% @ T=77 K < 0.1% @ T=300 K	Limited routing and system impedance
Non-Adjacent ROIC Pixel Crosstalk	< 0.1% @ T=77 K < 0.1% @ T=300 K	Limited routing and system impedance
Minimum Window Size and Resolution	≥ 16 columns x 8 Rows ≥ 32 columns x 8 Rows ≥ 64 columns x 8 Rows	4 Output Mode 8 Output Mode 16 Output Mode
Die Size	20.99 mm x 22.54 mm	Fit within exposure field
Pad Layout	Maximize commonality with ISC0404	