

# **ISC0903: 320 x 256 30µm Two Color ROIC**

## **Specification January 13, 2012**

- **Version 1.00: January 26, 2010**
  - Initial Release
- **Version 1.10: August 27, 2010**
  - Specification updated to reflect final design implementation
- **Version 1.11: January 13, 2012**
  - Removed markings for public release

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# FLIR ISC0903

## 320 x 256, 30µm ROIC

### ISC0903 Specification and Requirements Review (1 of 5)

ROIC PARAMETER	SPECIFICATION REQUIREMENT	COMMENTS
Array Configuration	320 x 256	
Pixel Pitch in Columns (320)	30µm	
Pixel Pitch in Rows (256)	30µm	
Input Polarity	Selectable P-on-N (Current Flows into Inputs) & N-on-P (Current Flows out of Inputs)	Color Selectable on a Per frame basis SLS, InSb, InGaAs, HCT
Detector Bond Pad	1 (6µm x 6µm) pad opening per pixel plus detector common pad ring around cell array	One indium bump connection per pixel. Additional detector common pad ring of 6 pixels around the array of 320x256 for a total array of 332x268. Maintain the same detector interface (pitch, array size, detector common ring size, hybridization targets) as the ISC9705.

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Test Detector Pads	4 pads to test individual detectors	Maintain the same pixel locations as the ISC9705
Input Configuration	Direct Injection (DI)	
Core Multiplexing Configuration	Voltage Mode	
Detector Impedance (RrAd) at 77K	$> 1 \times 10^3$ (Ohm-cm <sup>2</sup> )	Impedance at reverse bias operating point. Used for Performance Analysis, Prediction and Simulation.

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### ISC0903 Specification and Requirements Review (2 of 5)

ROIC PARAMETER	SPECIFICATION REQUIREMENT	COMMENTS												
Detector Capacitance	≤ 0.6pF	Used for Performance Analysis, Prediction, and Simulation Estimated												
Temperature of Operation	65K-300K	Room Temperature Operation Will Have Reduced Performance												
Input Biases	VDETCOM 0-5.5V VPOS 5.5V VPOSOUT 5.5V VPD 5.5V  VOUTREF 1.55V – 4N VNEG 0.0V VNEGOUT 0.0V VND 0.0V	Detector Common (optional) Analog Positive Output Positive Digital Positive Analog Reference, P-on-N 155V, N-on-P 4.N Analog Negative Output Negative Digital Negative												
Input Clocks	<table border="1"> <thead> <tr> <th>Name</th> <th>Vhigh to Vlow</th> </tr> </thead> <tbody> <tr> <td>CLK</td> <td>VPD to VND</td> </tr> <tr> <td>LSYNC</td> <td>VPD to VND</td> </tr> <tr> <td>FSYNC</td> <td>VPD to VND</td> </tr> <tr> <td>DATA</td> <td>VPD to VND RESET</td> </tr> <tr> <td>B</td> <td>VPD to VND</td> </tr> </tbody> </table>	Name	Vhigh to Vlow	CLK	VPD to VND	LSYNC	VPD to VND	FSYNC	VPD to VND	DATA	VPD to VND RESET	B	VPD to VND	
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Input Clock: Rise and Fall	10% to 90% in 10nS	
Outputs	Selectable 1, 2, or 4 with Reference Output	
Output Interface	$\geq 100k$ Ohms $\geq 12$ pF	12pF includes capacitive load up to and including wire-bond to ROIC pad

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### ISC0903 Specification and Requirements Review (3 of 5)

ROIC PARAMETER	SPECIFICATION REQUIREMENT	COMMENTS
Output Voltage Swing	2.5V ± 0.2V (Baseline P-on-N – 1.55V ± 0.1V)	Default settings -2.5V ± 0.2V typical output range at 77K Estimated range for 0.8V reverse detector bias Output swing dependent on reverse bias
Power (12.5MHz output data rate and T=77K unless otherwise noted)	4 Outputs ≤ 150mW 1 Outputs ≤ 60mW 60Hz	4 Outputs power assumes 6.25MHz clk 1 Outputs power assumes ~3MHz clk and adjusted power bits
Control Register Functions	Programmable Test 1/0 Anti-Blooming Control Power Control Master Current Detector Bias Adj. Invert/Revert Windowing (programmable size and position) 1, 2, or 4 Outputs Reference Output Enable Adjustable Timing Edges Global Reset Pixel Color Select	

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Programmable Test	Test Row Input Unit Cell Test Injection VET Circuit	
Detector Bias Adjust (P on N)	0mV to -800mV Adjustment @ nominal current (1nA)	-8mV bit bias control per color
Detector Bias Adjust (N on P)	0mV to +800mV Adjustment @ nominal current (1nA)	-8mV bit bias control per color
Detector Bias Uniformity	< 20mV 1-σ	Dependent on Process Dependent on Process Vt Uniformity Measured ISC9705 1-sigma of approximately 7mV, expect similar performance from ISC0903

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### ISC0903 Specification and Requirements Review (4 of 5)

ROIC PARAMETER	SPECIFICATION REQUIREMENT	COMMENTS
Integration Mode	Snap Shot ITR & WR	Integrate one color per frame
Integration Time	> 100µs to 0.9*full frame Adjustable on a per frame basis	For 240HZ → 4.167ms full frame → 3.75ms max tint Lowest Tint estimated it is possible to program Tint to <100µs, but integrated output may be nonlinear and limited.
Total Input Current Min Nominal Max	20pA 1 nA 10nA	Simulation Range includes signal and dark current
Input Charge Handling	18 x 10 <sup>6</sup> carriers	Can reduce well size with minimal layer changes
Non-Linearity	< ±2% from least squares line fit	Output Voltage vs. Tint Max Dev. from least squares fit over 15% to 85% of full range



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Noise	-80dB of Full Well (Input Referred) At Maximum Readout Rate	Without Detector or System Noise ROIC Noise in dB defined as $20 \cdot \log(\text{noise } e^- / \text{full well } e^-)$
Column Output Order-4 Output A  Output D	Column 0,4 316 Column 3,7 319	Four Output Mode Normal Readout Direction

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### ISC0903 Specification and Requirements Review (5 of 5)

ROIC PARAMETER	SPECIFICATION REQUIREMENT	COMMENTS
Invert / Revert	Reverse Order of Rows and/or Columns	Select using Control Register
Temperature Sensor	0.7V ± 0.05V @ 300K 1.070V ± 0.05V at 77K	Test/Temp Pad
Full Frame Rate Pixel Rate 12.5MHz & T=77K unless otherwise noted	4 Output ::?: 240 FPS 2 Output ::?: 120 FPS 1 Output ::?: 60 FPS	625MHz ISC0903 input clock For 256x256 windowed array
Data Valid / Settling Time	Settle to 0.1% @ T=77K in 65ns	12pF // 100k ohm load Default power settings
Adjacent ROIC Pixel Crosstalk	< 0.1% @ T=77K ----- <1% (@, T =300K	Limited routing and system impedance
Non-Adjacent ROIC Pixel Crosstalk	< 0.1% @ T=77K 4 output ----- < 1% @ T=300K 4 output	Limited routing and system impedance

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Color ROIC Pixel Crosstalk	<0.1% @ T=77K <1% @ T=300K	Limited routing and system impedance
Minimum Window Size and Resolution	≥ 4 columns x 4 Rows ≥ 8 columns x 4 Rows ≥16 columns x 4 Rows	1 Output Mode 2 Output Mode 4 Output Mode
Die Size	12.50mm x 12.50mm	To edge of scribe lane Goal to match ISC9705 die size of 11.39mm x 10.69mm for dewar compatibility
Pad Layout	Maximizing commonality with ISC9705	Match with ISC9705 as much as practical given the extra functionality of the ISC0903