Version 100 – initial release Nov. 2004 for version 100 of the ROIC design
Version 200 – updated release per version 200 of the ROIC design – July 2005

ISC0704
320 x 256, 30 um ROIC

Specification
and Requirements

ISC0704 Specification and Requirements Review (2 of 4)

ROIC PARAMETER	SPECIFICATION REQUIREMENT	COMMENTS	Page #	PROJECTED COMPLIANCE
Array Configuration	320 x 256	Compatible with ISC9705/0209 detectors Need to read out 320 x 240	273	"
Pixel Pitch in Columns (320)	30um		274-275	"
Pixel Pitch in Rows (256)	30um		274-275	"
Input Polarity	P-on-N (Current Flows into Inputs)	InSb	51	"
Input Configuration		Direct Injection (DI)	51	"
Core Multiplexing Configuration		Voltage Mode	85	"
Detector Impedance (RoAd) at 77K	> $2x10^4$ (Ohm-cm^2)	Used for Performance Analysis, Prediction and Simulation	58	"
Detector Capacitance	$\leq$ 0.2pF	Used for Performance Analysis, Prediction and Simulation	58	"
Temperature of Operation	77K	All Requirements Specified for 77K. Room Temperature Operation Will Have Reduced Performance.	--	"

ISC0704 Specification and Requirements Review (2 of 4)

ROIC PARAMETER	SPECIFICATION REQUIREMENT	COMMENTS	Page #	PROJECTED COMPLIANCE
Input Biases	VDET_ADJ 0V – 3.6V VPOS 3.6V VPOSOUT 3.6V VPD 3.6V VNEG 0.0V VNEGOUT 0.0V VND 0.0V VOUTREF 1.0V	Detector Common Analog Positive Output Positive Digital Positive Analog Negative Output Negative Digital Negative Analog Reference (Optional: Internal or external reference)	292	"
Input Clocks	Name Vhigh to Vlow CLK VPD to VND LSYNC VPD to VND FSYNC VPD to VND DATA VPD to VND RESET_B VPD to VND	 Master Clock Line Sync Frame Sync (Integ. Control) Mode Control (Optional) Master Reset (Optional)	292	"
Input Clock Rise and Fall	10% to 90% in 10nS		291	"
Outputs	1 with Reference Output	Reference output selectable	292	"
Output Interface	≥ 100k Ohms ≤ 10 pF		292	"

Output Voltage Swing	2.2V ± 0.2V (Baseline at 1.0V ± 0.1V)		140, 144	"

ISC0704 Specification and Requirements Review (3 of 4)

ROIC PARAMETER	SPECIFICATION REQUIREMENT	COMMENTS	Page #	PROJECTED COMPLIANCE
Power (6MHz output data rate)	≤ 20 mW	Goal ≤ 10mW	153	"
Control Register Functions	Programmable Test I/O Anti-Blooming Control Master Current Detector Bias Adjust Reference Output Enable Global Reset	Optional use. Not required if chip is operated using default settings.	199	"
Integration mode	IWR		19	"
Programmable Test	Test Row Input Unit Cell Test Injection VET Circuit		175	"
Detector Bias Adjust	100mV to -500mV Adjustment @ nominal current (1nA)	VDET_ADJ pad provides additional analog bias control	121-127	"

ISC0704 Specification and Requirements Review (4 of 4)

ROIC PARAMETER	SPECIFICATION REQUIREMENT	COMMENTS	Page #	PROJECTED COMPLIANCE
Input Current Nominal	≈ 0.5 nA	Used for simulations	55	"
Input Charge Handling	Option 1 ≥ 25 x 10^6 carriers Option 2 ≥ 18 x 10^6 carriers	Option 1 target = 30 x 10^6 carriers Option 2 target = 20 x 10^6 carriers	62	"
Non-Linearity	< ± 0.5% from least squares line fit	Output Voltage vs. Tint Max Dev. from least squares fit over 10% to 90% of full range	140, 144	Risk at 300K
Noise	-85dB of Full Well (Input Referred) At Maximum Readout Rate	Without Detector or System Noise	155-158	Risk
Output Order	Left to right, bottom to top	Pixel (0,0) in lower left corner	218	"
Full Frame Rate Pixel Rate 6MHz	≥ 60 FPS		30	"
Data Valid / Settling Time	Settle to 0.1% @ T=77K in ≤ 120ns Settle to 0.8% @ T=300K in ≤ 120ns	10pF // 100k∧ load	114, 118	"
Adjacent ROIC Pixel Crosstalk	< 0.1% @ T=77K < 0.8% @ T=300K		171-173	"

Non-Adjacent ROIC Pixel Crosstalk	< 0.1% @ T=77K < 0.8% @ T=300K		171- 173	''
Die Size	11.39 mm x 10.69 mm	Final size (after dicing) same as ISC9705/0209	273	''