- Version 100 – March 1, 2005 – Initial release
- Version 200 – May 17, 2005 – updated power supply levels, output level and noise spec per ROIC design version 200

ISC0402
Standard 640x512, 20um ROIC
Specification and Requirements
May 17, 2005

FLIR ISC0402 - Standard 640x512, 20um ROIC

ROIC PARAMETER	SPECIFICATION REQUIREMENT	COMMENTS
Array Configuration	640 x 512	Compatible with ISC9901 array
Pixel Pitch in Columns (640)	20um	
Pixel Pitch in Rows (512)	20um	
Input Polarity	P-on-N (Current Flows into Inputs)	InSb, InGaAs, HCT, QWIP
Input Configuration		Direct Injection (DI)
Core Multiplexing Configuration		Voltage Mode
Detector Impedance (RoAd) at 77K	> $2x10^4$ (Ohm-cm^2)	Used for Performance Analysis, Prediction and Simulation
Detector Capacitance	□□□0.04pF	Used for Performance Analysis, Prediction and Simulation
Temperature of Operation	77K	All Requirements Specified for 77K. Room Temperature Operation Will Have Reduced Performance.

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ROIC PARAMETER	SPECIFICATION REQUIREMENT	COMMENTS
Input Biases	VDETCOM 5.5V VPOS 5.5V VPOSD 5.5V VPOSOUT 5.5V VPD 3.8V VNEG 0.0V VNEGOUT 0.0V VND 0.0V VREF 1.6V	Detector Common Analog Positive Level Shifter Positive Output Positive Digital Positive Analog Negative Output Negative Digital Negative Analog Reference (Optional: Internal or external reference)
Input Clocks	Name Vhigh to Vlow CLK VPD to VND LSYNC VPD to VND FSYNC VPD to VND DATA VPD to VND RESET_B VPD to VND	 Master Clock Line Sync Frame Sync (Integ. Control) Mode Control Master Reset
Input Clock Rise and Fall	10% to 90% in 10nS	
Outputs	Selectable 1, 2 or 4 with Reference Output	
Output Interface	$\geq$ 100k Ohms $\leq$ 18 pF	
Output Voltage Swing	3.0V +/-0.3V	~1.6V – 4.6V

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ROIC PARAMETER	SPECIFICATION REQUIREMENT	COMMENTS
Power (12.5MHz output data rate)	1 Output ≤ 50 mW 2 Outputs ≤ 63 mW 4 Outputs ≤ 89 mW	
Power (10.25MHz output data rate)	4 Outputs ≤ 75 mW 4 Outputs ≤ 50 mW (goal)	120FPS
Control Register Functions	Programmable Test I/O Anti-Blooming Control Power Control Master Current Detector Bias Adj. Invert/Revert Windowing (programmable size and position) 1, 2 or 4 Outputs Integration Mode (ITR, IWR, NDRO) Reference Output Enable Global Reset	
Programmable Test	Test Row Input Unit Cell Test Injection VET Circuit	
Detector Bias Adjust	100mV to -500mV Adjustment @ nominal current (1nA)	7 bit bias control

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ROIC PARAMETER	SPECIFICATION REQUIREMENT	COMMENTS
Input Current Nominal	≈ 0.5 nA	Used for simulations
Input Charge Handling	Option 1: ≥ 6 x 10^6 carriers Option 2: 3.0 ± 0.5 x 10^6 carriers	Goal > 10 x 10^6 carriers (Option 1)
Non-Linearity	< ± 0.5% from least squares line fit	Output Voltage vs. Tint Max Dev. from least squares fit over 10% to 80% of full range
Noise	TBD of Full Well (Input Referred) At Maximum Readout Rate	Without Detector or System Noise
Column Output Order-1 Output A	 Column 0,1,…,639	One Output Mode Normal Readout Direction
Column Output Order-2 Output A Output B	 Column 0,2,…,638 Column 1,3,…,639	Two Output Mode Normal Readout Direction
Column Output Order-4 Output A Output B Output C Output D	 Column 0,4,…,636 Column 1,5,…,637 Column 2,6,…,638 Column 3,7,…,639	Four Output Mode Normal Readout Direction
Invert / Revert	Reverse Order of Rows and/or Columns	Select using Control Register
Temperature Sensor	0.7V ± 0.05V @ 300K 1.070V ± 0.05V at 77K	Test/Temp Pad

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ROIC PARAMETER	SPECIFICATION REQUIREMENT	COMMENTS
Full Frame Rate Pixel Rate 12.5MHz	1 Output ≥ 30 FPS 2 Output ≥ 60 FPS 4 Output ≥ 120 FPS	Goal: 4 output ≥ 120FPS (Data rate ≤ 10.8MHz)
Data Valid / Settling Time	Settle to 0.1% @ T=77K in ≤ 55ns Settle to 0.8% @ T=300K in ≤ 55ns	18pF // 100kΩ load Default power settings
Adjacent ROIC Pixel Crosstalk	< 0.1% @ T=77K < 0.8% @ T=300K	
Non-Adjacent ROIC Pixel Crosstalk	< 0.1% @ T=77K < 0.8% @ T=300K	
Minimum Window Size	≥ 4 columns x 4 Rows ≥ 8 columns x 4 Rows ≥ 16 columns x 4 Rows	1 Output Mode 2 Output Mode 4 Output Mode
Die Size	15.74 mm x 14.77 mm	