FLIR ISC0002-1
640 x 512 NIR ROIC

Specification
October 16, 2009

Official Publication Date: Oct. 16, 2009

Document Revision History

- **Version 1.0 5/26/04**
  - ***Initial Release***
- **Version 1.10 4/15/05**
  - *correct high gain integration capacitor values*
- **Version 1.11 10/16/09**
  - *correct noise values, correct all cap values, remove ref. to -02 of the design*

General Description

- **High Performance CMOS ROIC for NIR Imaging Applications**
  - 640 x 512 Format, 25□m unit cell
  - Designed for P-on-N HgCdTe and InGaAs detectors
  - Derivative of ISC9803 (640 x 512) and ISC9809 (320 x 240) Standard ROICs
  - CTIA input circuit with selectable integration capacitors and selectable bandwidth
  - Snap shot integration either integrate while reading out or integrate then read out
  - Variable integration time plus Gated integration for pulsed laser applications
  - One Option of ISC0002 available
    - Option 1 (ISC0002-1) is optimized for imaging applications
- **Multiple operating modes controlled by serial data interface**
  - Windowing
  - Invert/revert pixel read out, interlaced or non-interlaced
  - Selectable number of outputs - 1, 2, or 4
  - Multiple read outs per integration period for astronomy applications
  - Adjustable internal bias supplies to control power dissipation
  - Input skimming
  - Default mode - 30 Hz frame rate, Interlaced 640 x 512 Window, high input gain (smallest C_{INT}), lowest input circuit bandwidth, 1 output - supports NTSC or PAL video timing

ISC0002 Specification and Requirements Review (1 of 6)

ROIC PARAMETER	SPECIFICATION REQUIREMENT	COMMENTS
Array Configuration	640 x 512	
Pixel Pitch In Columns (640)	25µm	
Pixel Pitch in Rows (512)	25µm	
Input Polarity	P-on-N	HgCdTe and InGaAs (will also support InSb)
Input Configuration	CTIA	
Core Multiplexing Configuration	Voltage Mode	
Detector Zero-Biased Impedance (R_oA_d) at 250Kelvin	> $1.0x10_7$ (Ohm-cm^2)	Used for Performance Analysis Prediction and Simulation
Detector Capacitance at 0.5volt Reverse Bias	≤ 0.05pF	Used for Performance Analysis Prediction and Simulation

ISC0002 Specification and Requirements Review (2 of 6)

ROIC PARAMETER	SPECIFICATION REQUIREMENTS	COMMENTS
Input Biases	VDETCOM 3.10 to 5.5V VPOS_CORE 5.5V VPOS 5.5V VPOSOUT 5.5V VPD 5.5V VREF 2.6 TO 3.15V VOUTREF 1.6V VNEG_CORE 0.0V VNEG 0.0V VNEGOUT 0.0V VND 0.0V	Detector Common (P-on-N) Analog Positive Supply Analog Positive Supply Output Positive Supply
Input Clocks	Name Vhigh to Vlow CLK VPD TO VND LSYNC VPD TO VND FSYNC VPD TO VND DATA VPD TO VND FIELD VPD TO VND RESET_B VPD TO VND	Master Clock Line Sync Frame Sync (Integ. Control) Mode Control Interlace Field Sync Master Reset Pin
Input Clock Rise and Fall	10% to 90% in 10nS	
Outputs	Selectable 1, 2, or 4 with Reference Output	
Output Interface	> 100K Ohms ≤ 25 pF	

Output Voltage Swing	> 2.5 V swing	Up to 2.6 volts (2.15v to 4.75v) May be limited by linearity and uniformity

ISC0002 Specification and Requirements Review (3 of 6)

ROIC PARAMETER	SPECIFICATION REQUIREMENTS	COMMENTS
Output Voltage Swing	< 225mW Single Output <325mW Four Output Mode at max frame rate	224.7mW Estimated 312mW Estimated Power controllable using external bias or on-chip DAC
Control Register Functions	Input skimming Power Control Integration Gain Select Bandwidth Limit Input Amp Integration/Read Out Mode Invert/Revert Format Window Size Window Position 1, 2, 4 Outputs Enable Reference Output Interlace Read Out Global Reset	Details given in Logic Section
Detector Bias Adjust	Externally Adjusted through VDETCOM or VREF voltages	
Nominal Operating Temperature	250 Kelvin	Also 80 Kelvin

ISC0002 Specification and Requirements Review (4 of 6)

ROIC PARAMETER	SPECIFICATION REQUIREMENTS	COMMENTS
Input Current Min Nominal Max	 0.01 pA 1.00 pA 50 nA	Simulation Range
Gain Control (C_{INT} Control	Rel. Gain Bit uV/e- Gain Max e- 0 64 49.0* 39K * 1 1.3 1.0 1.9M *Default Gain Setting	
Input Charge Handling	≈ 3.9x104 & 1.9x106 carriers (2.5fF& 122fF* @ 2.5V)	Low gain* - Cint effective varies over integration range
Transimpedance Non-Linearity	< ±0 5% from least squares line fit from 10% to 90% of the signal dynamic range	Output Voltage vs. Tint
Readout Noise Floor at 250Kelvin with Vbias = -0.5V C_d = 0.05pF $R_o A_d = 1x10^7$	Output Gain Bit / Input Noise / ISC0002-1 Noise e- 0 4480µV 70 1 853 μ V 656	~2.7uS Tint for ISC0002-1
Min Tint Special Short ITR Integration Mode	1µS	

ISC0002 Specification and Requirements Review (5 of 6)

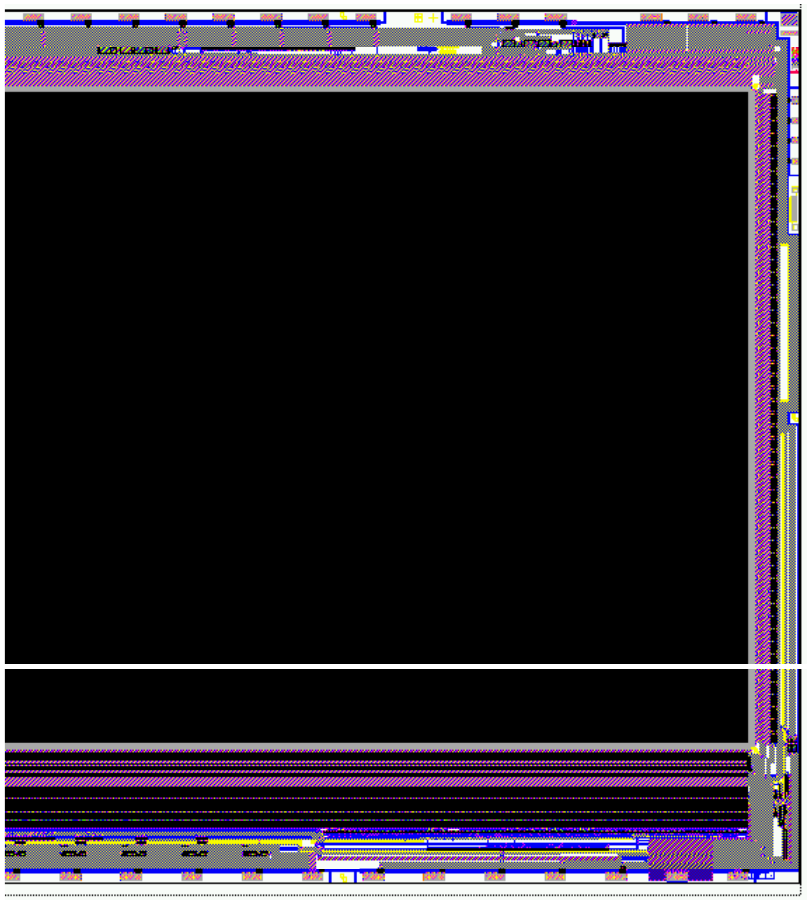
ROIC PARAMETER	SPECIFICATION REQUIREMENTS	COMMENTS
Column Output Order Output 1 Output 2 Output 3 Output 4	Column 0,4,8,12,…,636 Column 1,5,9,13,…,637 Column 2,6,10,14,…,638 Column 3,7,11,15,…,639	Four Output Mode Normal Readout Direction
Column Output Order Output 1 Output 2	Column 0,2,4,6,…,638 Column 1,3,5,7,…,639	Two Output Mode Normal Readout Direction
Column Output Order Output1	0,1,2,3,4,……..,639	Single Output Mode Normal Readout Direction
Invert / Revert	Reverse Order of Rows and/or Columns	Select using Control Register
Temperature Sensor	0.7V +/- 0.05V 300Kelvin	at Temp Sensor Pad

ISC0002 Specification and Requirements Review (6 of 6)

ROIC PARAMETER	SPECIFICATION REQUIREMENTS	COMMENTS
Frame Rate Pixel Rate 10MHZ	4 Output - 107 FPS 2 Output - 58 FPS 1 Output - 30 FPS	Reading out 640x480 (Non-Interlaced) at 5MHz Master C
Data Valid / Settling Time	Settle to 0.1% @ T=80K in < 70ns Settle to 0.39% @ T 250K **in < 70ns**	Output Load Cload = 25pf Rload = 100K
Adjacent Pixel Crosstalk	< 0.2% @ T=80K < 0.39% @ T=250K	
Non-Adjacent Pixel Crosstalk	< 0.1% @ T=80K < 0.2% @ T=250K	
Minimum Window Size (Max Frame Rate)	> 32 columns X 8 Rows > 64 columns X 8 Rows > 128 columns X 8 Rows	1 Output Mode (14.16KFPS) 2 Output Mode (14.16KFPS) 4 Output Mode (14.16KFPS)

The ISC0002 - Design Features

- 640 x 512 readout for P-on-N InGaAs, HgCdTe, InSb, Advanced Features
- Snapshot Mode Integration
- Flexible Integration Control
  - Integrate-While-Read
  - Integrate-Then-Read
- Variable Input Circuit Gain
- Vairable Input Circuit Bandwidth
- Input Skimming
- Windowing Readout, Selectable – 1, 2, or 4 Outputs with Reference Output
- Low Power, Simple Operation
- Detector Interface compatible with standard 640 ROIC – ISC9803.



ISC0002
640 x 512 ROIC Overview 1 of 2

- **640 x 512 array with 25μm x 25μm pixel pitch**

- **CTIA input circuit for P-on-N detectors (low background)**
  - Selectable integration capacitor, selectable input amplifier bandwidth, and input skimming
  - No image lag with CTIA input circuit even at very low input currents

- **Supports multiple integration/readout modes**
  - Snap shot integrate-while-read out
  - Snap shot integrate-then-read out, Snap shot integrate-then-read out for very short integration times
  - Multiple frame read out per integration period
  - Interlaced or non-interlaced read out
  - Integration controlled by frame sync (FSYNC) duty cycle

- **Variable integration time**
  - Integration time set by FSYNC pulse length and CLK period
  - Minimum integration time is approximately 5.4μsec (<3μsec for special gated integrate then read mode)
  - Maximum integration time is approximately the frame period

- **Voltage mode column multiplexer architecture**

ISC0002
640 x 512 ROIC Overview 2 of 2

- **Optional serial data interface (Control Register)**
  - Windowing
  - Selectable input circuit bandwidth
  - Power adjustment for frame rate compensation
  - Enable input skimming
  - Invert / Revert
  - 1,2, or 4 outputs
  - Enable reference output

- **Overrides when Control Register not used**
  - Power control
  - Integration capacitor selection
  - Input circuit bandwidth selection

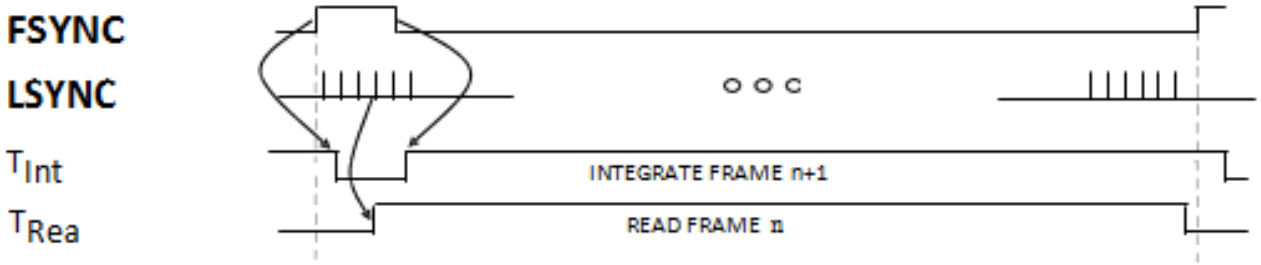
- **Interface**
  - 4 Clocks, reset pad, gain pad, bandwidth pad
  - 2 unique bias voltages
  - 1, 2, or 4 Outputs with optional reference output
  - Temperature sensor output

- **Maximum frame rate of 107Hz with 5MHz master clock**

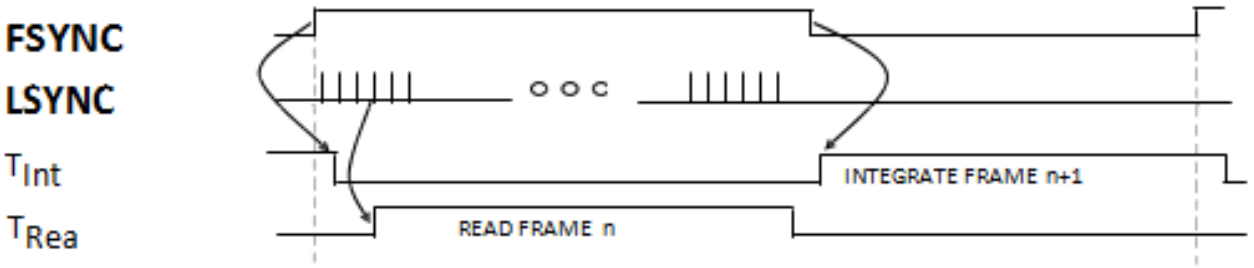
- 250Kelvin to 80Kelvin operating temperature
- Less than 70 electrons rms readout noise floor at 250Kelvin with detector capacitance ≤ 0.05pF in normal ITR mode

ISC0002
Integration Timing (1 of 2)

- Integrate While Read: $T_{Frame} = T_{Read}$



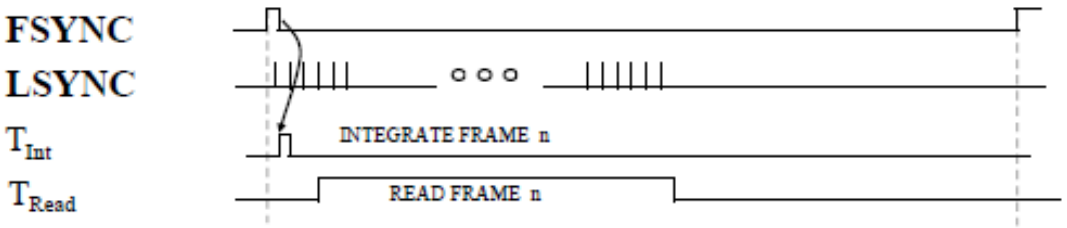
- Normal IntegrateThen Read: $T_{Frame} \sim T_{Read} + T_{Int}$



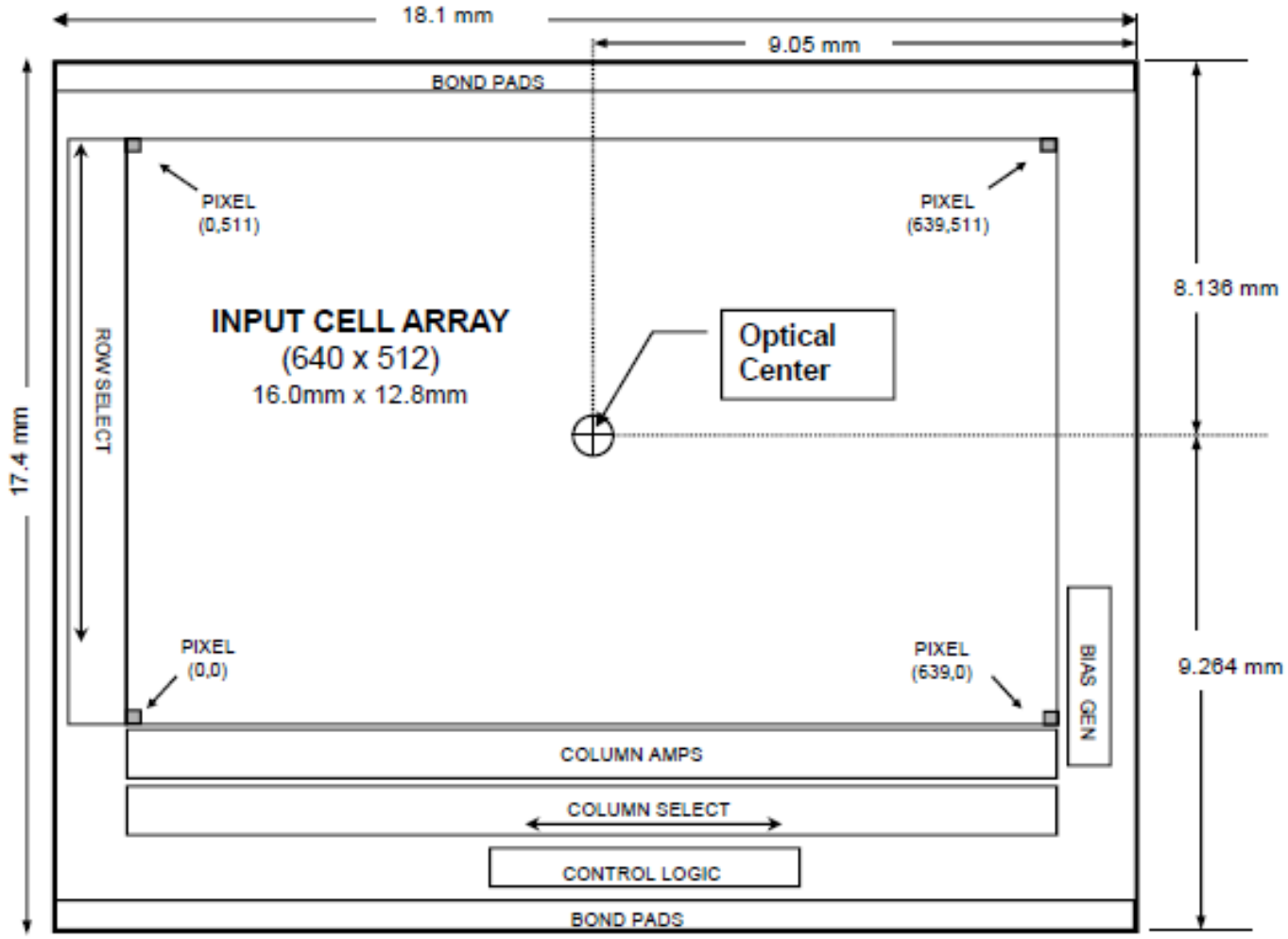
ISC0002
Integration Timing (2 of 2)

- Special Integrate Then Read: $T_{Frame} \sim T_{read} + T_{Int}$

Special ITR



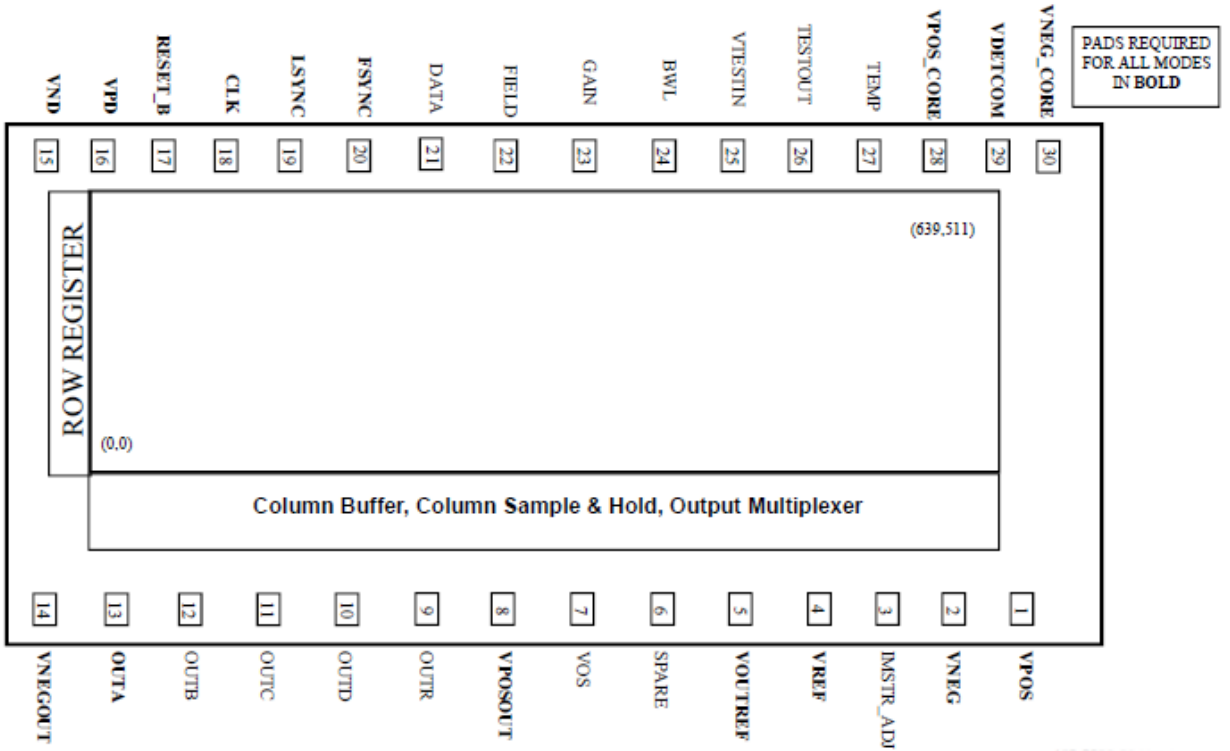
ISCOOO2 ROIC
Floorplan



ISC0002
Layout Summary

- AMI Standard 0.5µm process (updated 2/11/02)
  - Converted from 0.6 µm process on 2/11/02
- Die Size = 18.1mm x 17.4mm
  - As Measured to Edge of Scribe Lane
- 200mm (8”) Wafers (updated 2/11/02)
  - Estimate 78 Die / Wafer
  - 180µm Scribe Lane in X and Y Directions
  - 625 +/ 25µm Wafer Thickness
  - BULK Starting Material
- Input Cell Pad Opening:
  - 5.0µm x 5.0µm

ISC0002 Pad Placement



ISC002 Interface Definition
Supplies, Biases, and Clocks

ISC0002 Interface

BIAS	VOLTAGE	CURRENT	PK CURRENT	GAIN TO OUTPUT	
VPOS	5.5V	< 15 mA	< 60mA	<0.3	Positive Analog Supply
VNEG	0V	< 15 mA	< 60mA	<1	Negative Analog Supply & Substrate
VPOS_CORE	5.5V	<80mA	<100mA	<1	Positive Analog Supply
VNEG_CORE	0V	<80mA	<100mA	<1	Negative Analog Supply
VPOSOUT	5.5V	< 25mA	< 80mA	<0.1	Output Driver Positive Supply
VNEGOUT	0V	< 25mA	< 80mA	<0.3	Output Driver Negative Supply
VPD	5.5V	< 15mA	< 110mA	<0.1	Logic Positive Supply
VND	0V	< 15mA	< 110mA	<0.1	Logic Negative Supply
VDETCOM	2.7-5.5V	< 20mA	< 120mA	<15	Detector Substrate Connection
VOUTREF	1.6V	<1mA	<80mA	<1	Output Reference Level
VREF	2.2-3.2V	< 1mA	< 20mA	<15	CTIA Amplifier Reference Supply

Note: 0V and 5.5V Supplies May be Combined After Capacitive Bypass
Conditions = SPECIAL ITR , 4 Output Mode, Highest Power Mode

CLOCKS	LEVELS	LOAD	RISE/FALL	
CLK	0V - 5.5V	< 20pF	< 10nsec	Master Clock - Output on Half Clock Cycles
FSYNC	0V - 5.5V	< 10pF	< 10nsec	Frame Sync - Controls Frame Start & Integration Time
LSYNC	0V - 5.5V	< 10pF	< 10nsec	Line Sync - Controls Line Readout Timing
DATA	0V - 5.5V	< 10pF	< 10nsec	Data Word Input - Programs Chip Function Registers
FIELD	0V - 5.5V	< 10pF	< 10nsec	Field Sync - Controls Interlaced Field Readout
RESET_B*	0V - 5.5V	< 10pF	< 10nsec	Resets Digital Registers & Latches when a logic "0" is applied, Normally pulled up to logic "1"
OUTPUTS	LEVELS	LOAD	SETTLE	
OUTA	1.6V to 4.8V	25pF // 100K	< 70nsec to 0.1%	T=80K, 0.39% for t=300K Output A used in Single Output Mode
OUTB	1.6V to 4.8V	25pF // 100K	< 70nsec to 0.1%	T=80K, 0.39% for t=300K Output A and B used in Two Output Mode
OUTC	1.6V to 4.8V	25pF // 100K	< 70nsec to 0.1%	T=80K, 0.39% for t=300K Output A, B, C, and D used in Four Output Mode
OUTD	1.6V to 4.8V	25pF // 100K	< 70nsec to 0.1%	T=80K, 0.39% for t=300K Output A, B, C, and D used in Four Output Mode
OUTR	1.6V	25pF // 100K		Reference for Common Mode Output

MISC	VOLTAGE	
IMSTR_ADJ *	0V - 5.5V	Power Override
TEMP	0V - 5.5V	Temp Monitor
GAIN *	0V - 5.5V	Gain Select
BWL *	0V - 5.5V	Bandwidth Select
VOS	1.6V - 5.5V	Variable Offset/Skimming Control Voltage
TESTOUT	0V - 5.5V	Test Mode Output
VTESTIN	0V - 5.5V	Test Mode Control Signal
TESTDET(1-4)	5.5V	Test Detector Access
SED_L	5.5V	Test Single Element Detector Pad on Left side of ROIC
SED_R	5.5V	Test Single Element Detector Pad on Right side of ROIC

* Also Addressable through Control Register (along with Windowing and Readout Format Invert/Revert)

ISC0002 ROIC
Suggested I/O Interface

PAD Number	PAD	I/O Resistance (Ohms)	I/O Inductance (nH)	I/O Capacitance (F)
1	VPOS	≤ 5	≤ 50	≥ 5u
2	VNEG	≤ 0.5	≤ 15	NA
3	IMSTR_ADJ	≤ 50	≤ 50	N.C.
4	VREF	≤ 1	≤ 15	≥ 5u
5	VOUTREF	≤ 5	≤ 50	≥ 5u
6	SPARE	N.C.	N.C.	N.C.
7	VOS	≤ 1	≤ 50	≥ 5u
8	VPOSOUT	≤ 5	≤ 50	≥ 5u
9	OUTR	≤ 5	≤ 50	≤ 25p
10	OUTD	≤ 5	≤ 50	≤ 25p
11	OUTC	≤ 5	≤ 50	≤ 25p
12	OUTB	≤ 5	≤ 50	≤ 25p
13	OUTA	≤ 5	≤ 50	≤ 25p
14	VNEGOUT	≤ 5	≤ 50	NA
15	VND	≤ 2	≤ 50	NA
16	VPD	≤ 2	≤ 50	≥ 5u
17	RESET_B	≤ 25	≤ 50	NA
18	CLK	≤ 25	≤ 50	NA
19	LSYNC	≤ 25	≤ 50	NA
20	FSYNC	≤ 25	≤ 50	NA
21	DATA	≤ 25	≤ 50	NA
22	FIELD	≤ 25	≤ 50	NA
23	GAIN	≤ 50	≤ 50	NA
24	BWL	≤ 50	≤ 50	NA
25	VTESTIN	N.C	N.C.	N.C.
26	TESTOUT	N.C.	N.C.	N.C.
27	TEMP	≤ 50	≤ 50	≥ 0.5N
28	VPOS_CORE	≤ 0.1	≤ 15	≥ 5u
29	VDETCOM	≤ 0.1	≤ 15	≥ 5u
30	VNEG_CORE	≤ 0.1	≤ 15	NA

Values for
Worst case
10MHz
4-Output Mode